FIG. 1

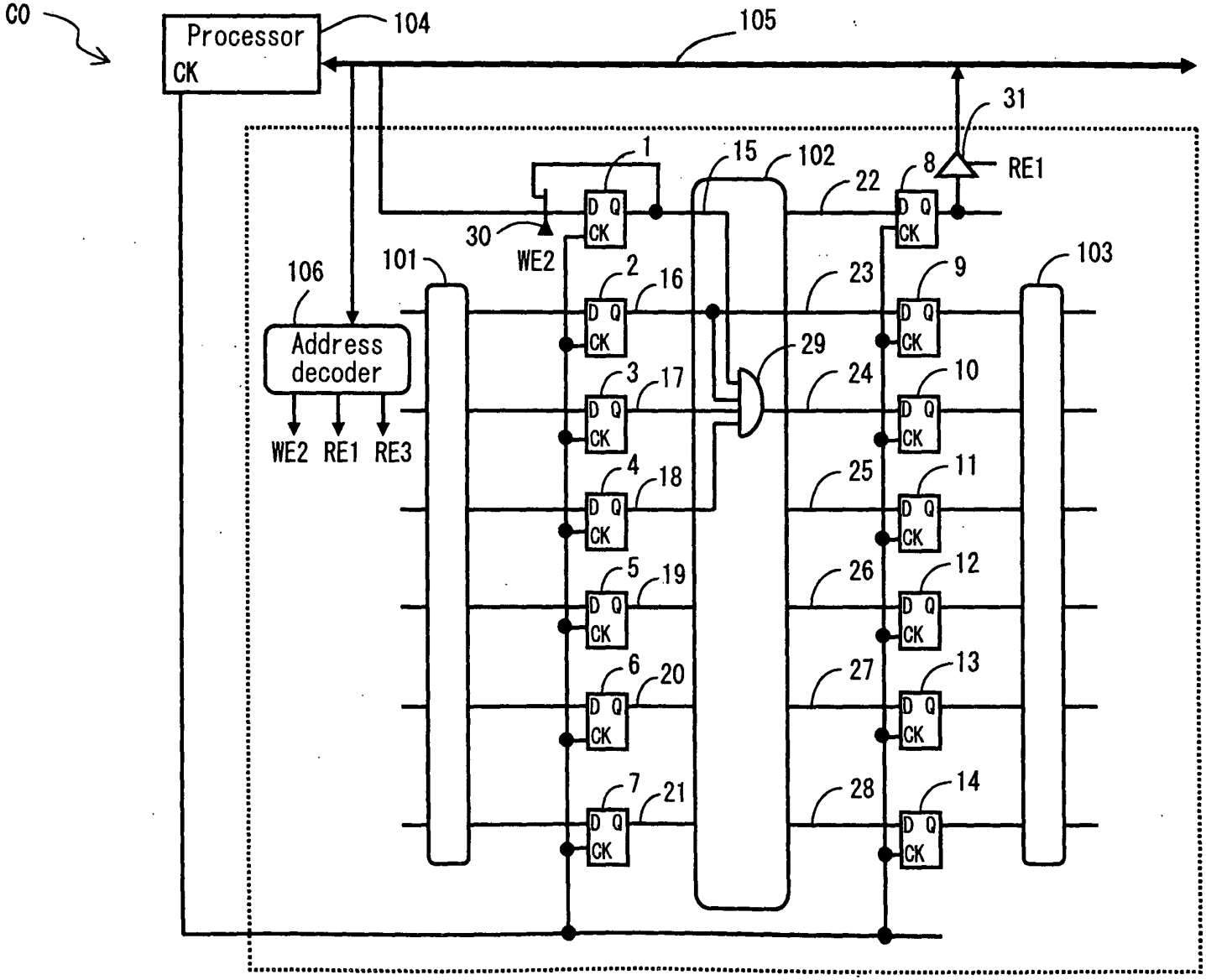

C0
Processor
CK
104
105
31
RE1
1
15
102
22
8
30
WE2
101
106
Address decoder
WE2 RE1 RE3
2
16
23
9
103
29
3
17
24
10
4
18
25
11
5
19
26
12
6
20
27
13
7
21
28
14
D Q
CK

FIG. 2

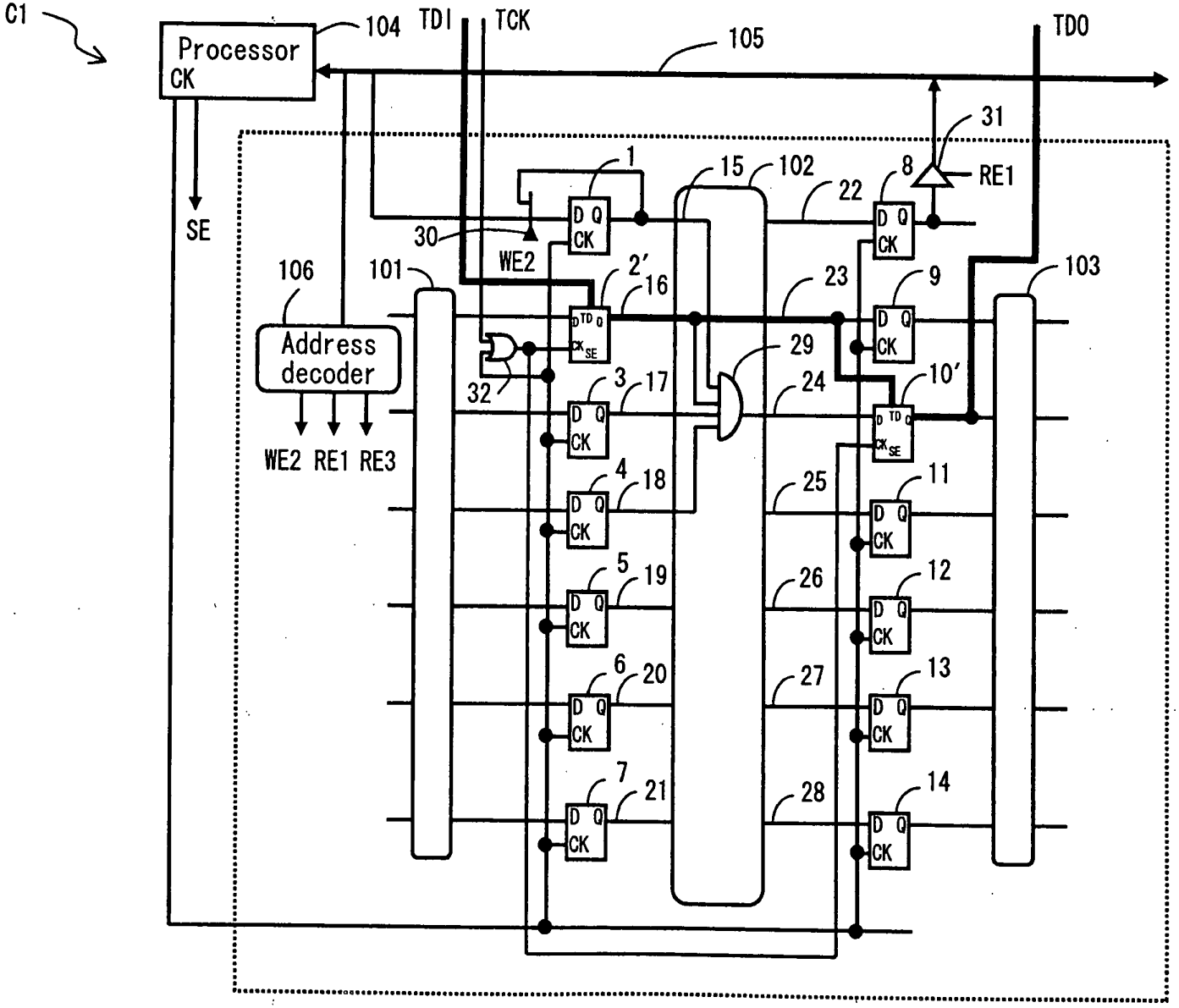

C1
Processor
CK
104
TDI
TCK
105
TDO
SE
31
RE1
8
22
1
15
102
30
WE2
2'
16
106
101
Address
decoder
WE2 RE1 RE3
23
9
103
29
32
3
17
24
10'
4
18
25
11
5
19
26
12
6
20
27
13
7
21
28
14
D Q
CK
TD
SE

FIG. 3A

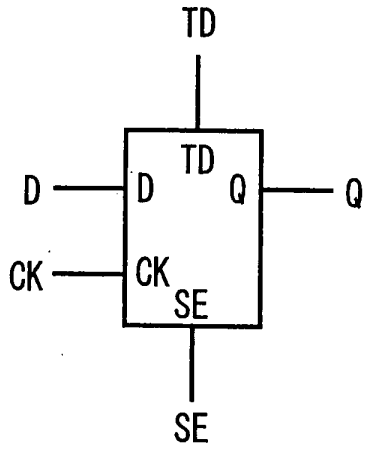


FIG. 3B

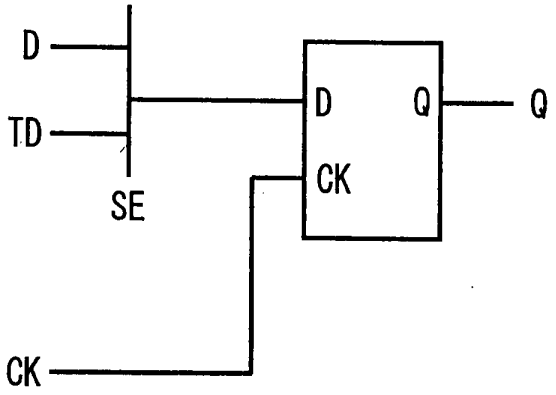


FIG. 4

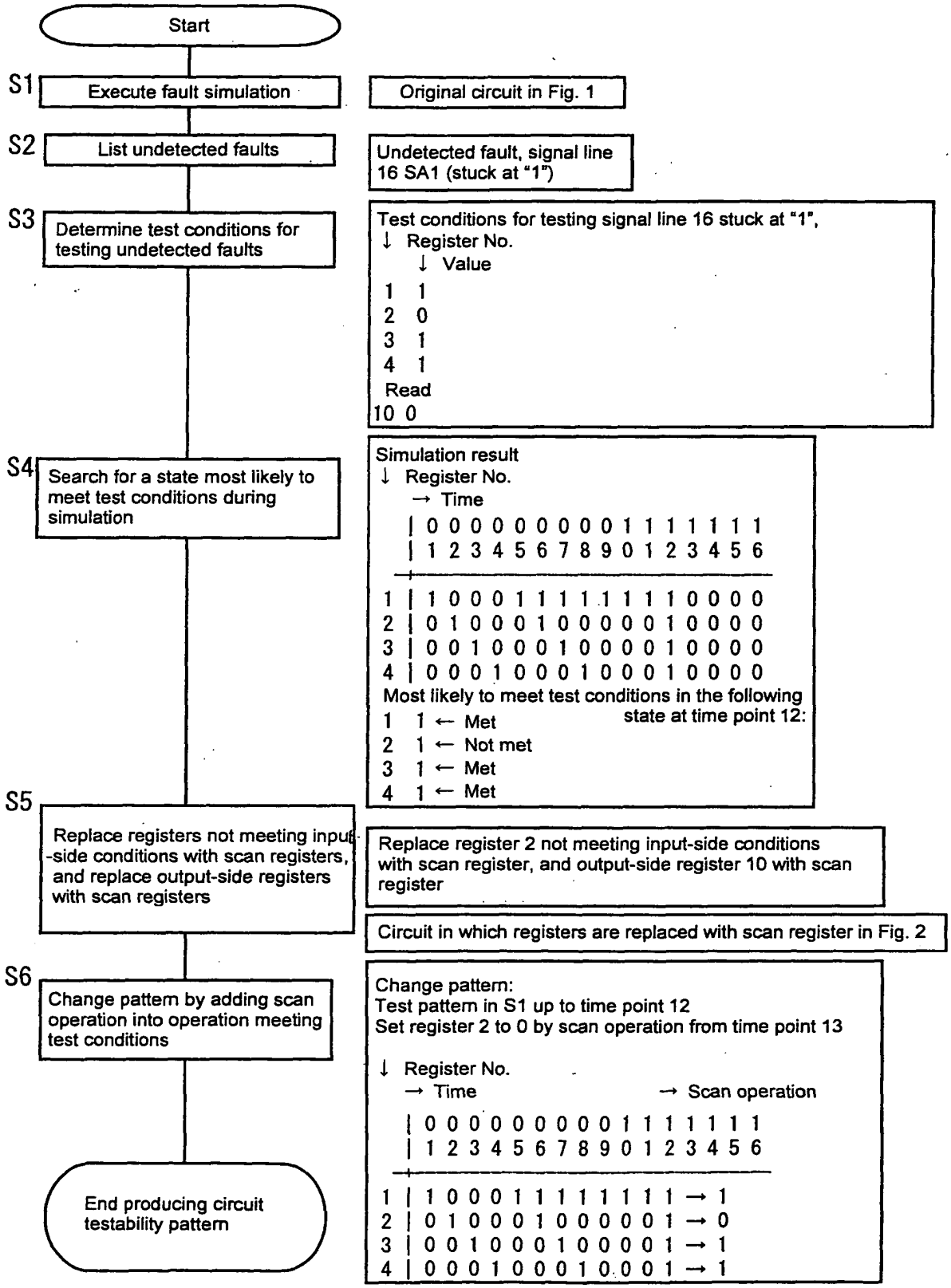

Start
S1
Execute fault simulation
Original circuit in Fig. 1
S2
List undetected faults
Undetected fault, signal line 16 SA1 (stuck at "1")
S3
Determine test conditions for testing undetected faults
Test conditions for testing signal line 16 stuck at "1",
↓ Register No.
↓ Value
1 1
2 0
3 1
4 1
Read
10 0
S4
Search for a state most likely to meet test conditions during simulation
Simulation result
↓ Register No.
→ Time
| 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1
| 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6
1 | 1 0 0 0 1 1 1 1 1 1 1 1 0 0 0 0
2 | 0 1 0 0 0 1 0 0 0 0 0 1 0 0 0 0
3 | 0 0 1 0 0 0 1 0 0 0 0 1 0 0 0 0
4 | 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 0
Most likely to meet test conditions in the following state at time point 12:
1 1 ← Met
2 1 ← Not met
3 1 ← Met
4 1 ← Met
S5
Replace registers not meeting input-side conditions with scan registers, and replace output-side registers with scan registers
Replace register 2 not meeting input-side conditions with scan register, and output-side register 10 with scan register
Circuit in which registers are replaced with scan register in Fig. 2
S6
Change pattern by adding scan operation into operation meeting test conditions
Change pattern:
Test pattern in S1 up to time point 12
Set register 2 to 0 by scan operation from time point 13
↓ Register No.
→ Time
→ Scan operation
| 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1
| 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6
1 | 1 0 0 0 1 1 1 1 1 1 1 1 → 1
2 | 0 1 0 0 0 1 0 0 0 0 0 1 → 0
3 | 0 0 1 0 0 0 1 0 0 0 0 1 → 1
4 | 0 0 0 1 0 0 0 1 0 0 0 1 → 1
End producing circuit testability pattern

FIG. 5

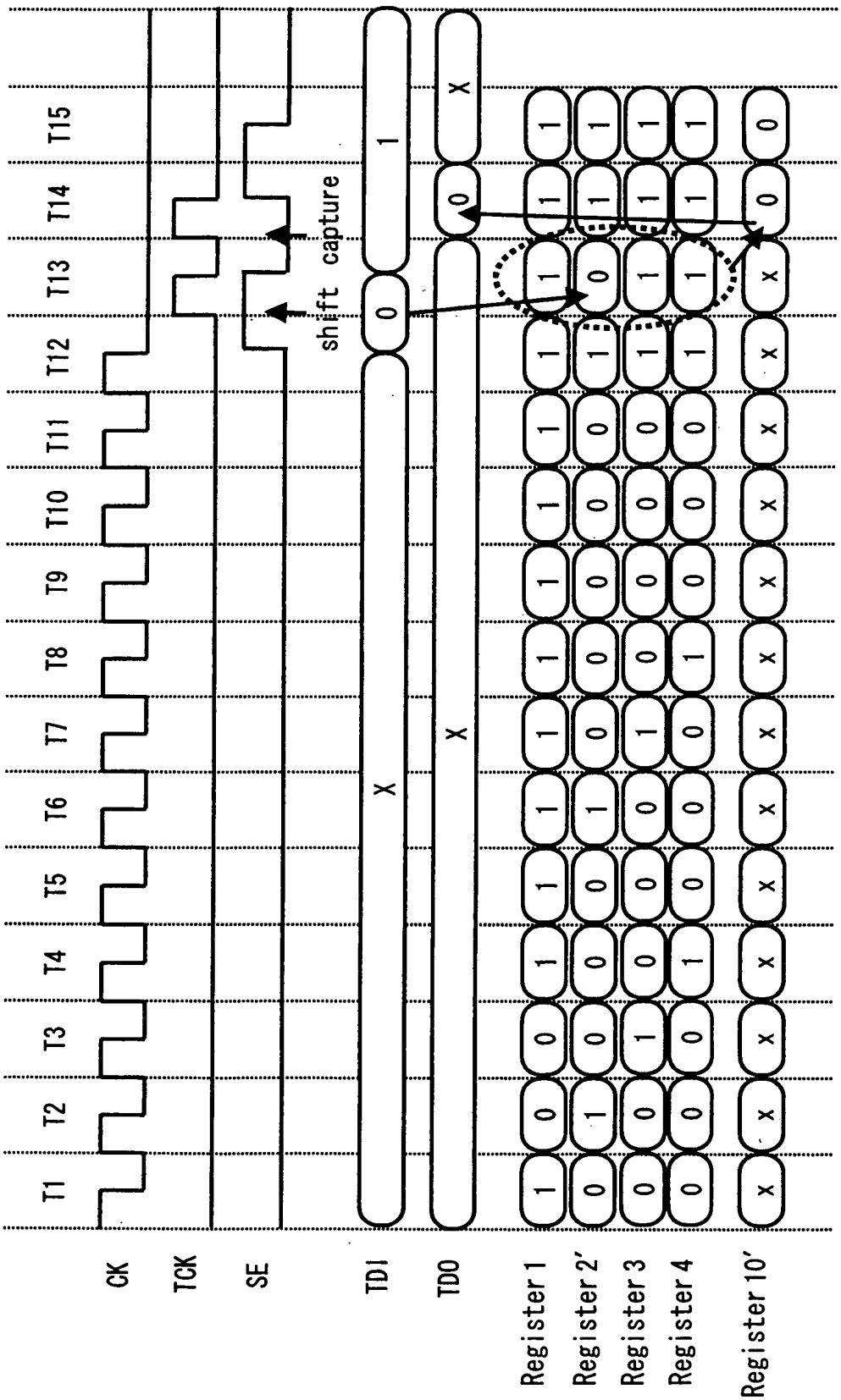

T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
CK
TCK
SE
TDI
TDO
shift capture
Register 1
Register 2'
Register 3
Register 4
Register 10'

FIG. 6

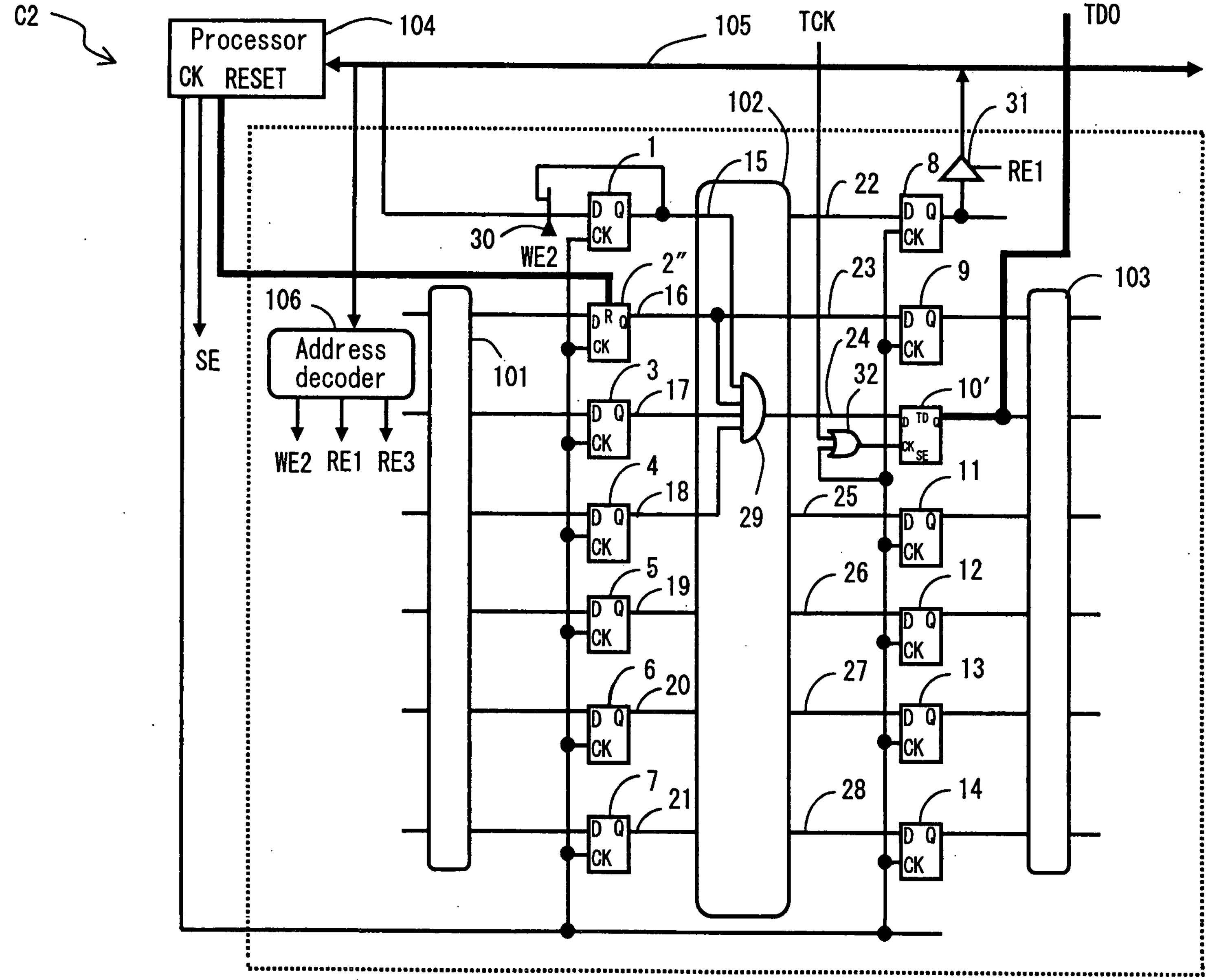

C2
Processor
CK RESET
104
105
TCK
TDO
SE
106
Address decoder
WE2 RE1 RE3
101
102
103
1
2″
3
4
5
6
7
8
9
10′
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
WE2
31
RE1
32
D Q
CK
D R Q
D TD Q
CK SE

FIG. 7

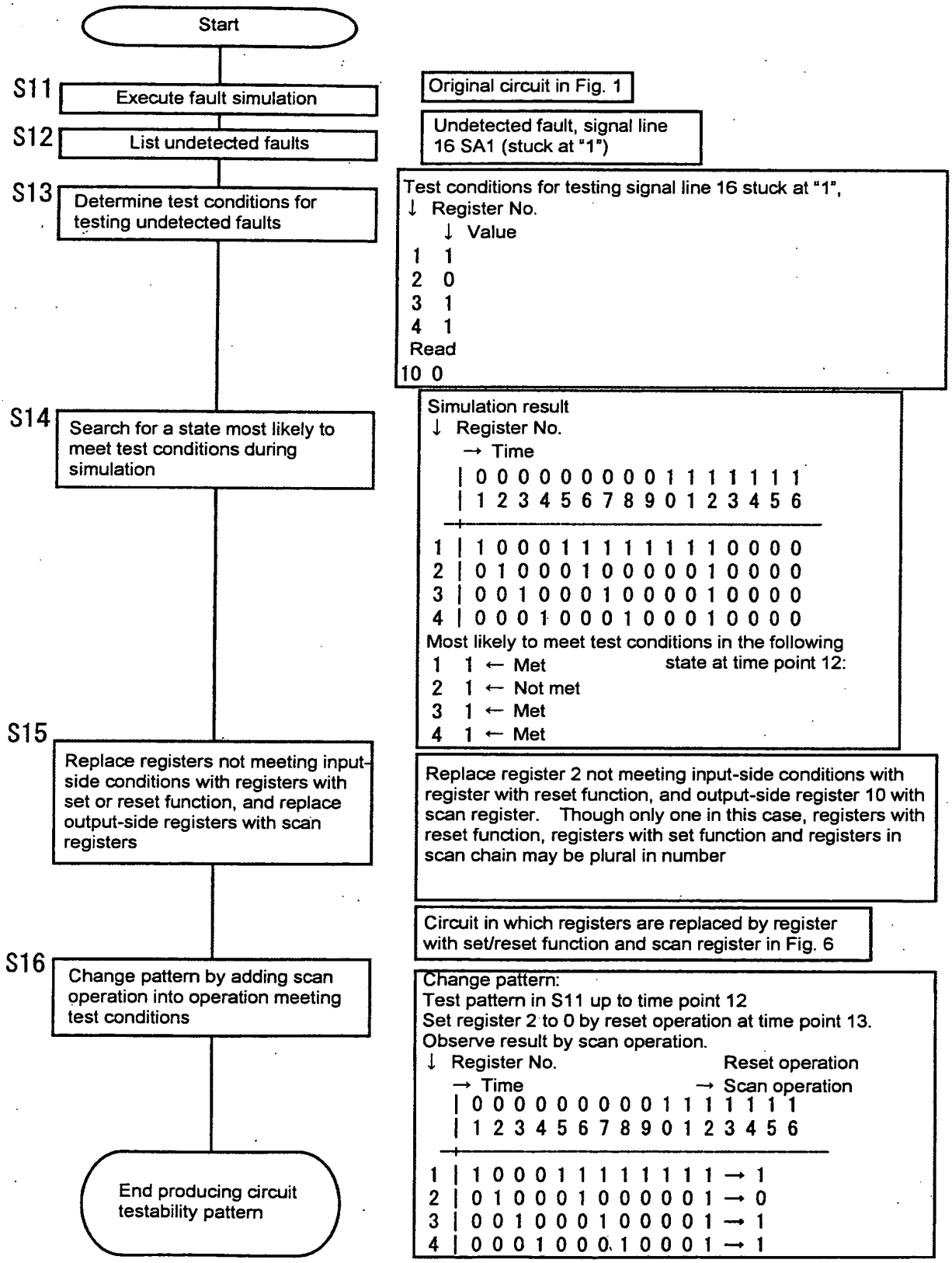

Start
S11
Execute fault simulation
S12
List undetected faults
S13
Determine test conditions for testing undetected faults
S14
Search for a state most likely to meet test conditions during simulation
S15
Replace registers not meeting input-side conditions with registers with set or reset function, and replace output-side registers with scan registers
S16
Change pattern by adding scan operation into operation meeting test conditions
End producing circuit testability pattern
Original circuit in Fig. 1
Undetected fault, signal line 16 SA1 (stuck at "1")
Test conditions for testing signal line 16 stuck at "1",
↓ Register No.
↓ Value
1 1
2 0
3 1
4 1
Read
10 0
Simulation result
↓ Register No.
→ Time
| 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1
| 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6
1 | 1 0 0 0 1 1 1 1 1 1 1 1 0 0 0 0
2 | 0 1 0 0 0 1 0 0 0 0 0 1 0 0 0 0
3 | 0 0 1 0 0 0 1 0 0 0 0 1 0 0 0 0
4 | 0 0 0 1 0 0 0 1 0 0 0 1 0 0 0 0
Most likely to meet test conditions in the following state at time point 12:
1 1 ← Met
2 1 ← Not met
3 1 ← Met
4 1 ← Met
Replace register 2 not meeting input-side conditions with register with reset function, and output-side register 10 with scan register. Though only one in this case, registers with reset function, registers with set function and registers in scan chain may be plural in number
Circuit in which registers are replaced by register with set/reset function and scan register in Fig. 6
Change pattern:
Test pattern in S11 up to time point 12
Set register 2 to 0 by reset operation at time point 13.
Observe result by scan operation.
↓ Register No.
→ Time
Reset operation
→ Scan operation
| 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1
| 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6
1 | 1 0 0 0 1 1 1 1 1 1 1 1 → 1
2 | 0 1 0 0 0 1 0 0 0 0 0 1 → 0
3 | 0 0 1 0 0 0 1 0 0 0 0 1 → 1
4 | 0 0 0 1 0 0 0 1 0 0 0 1 → 1

FIG. 8

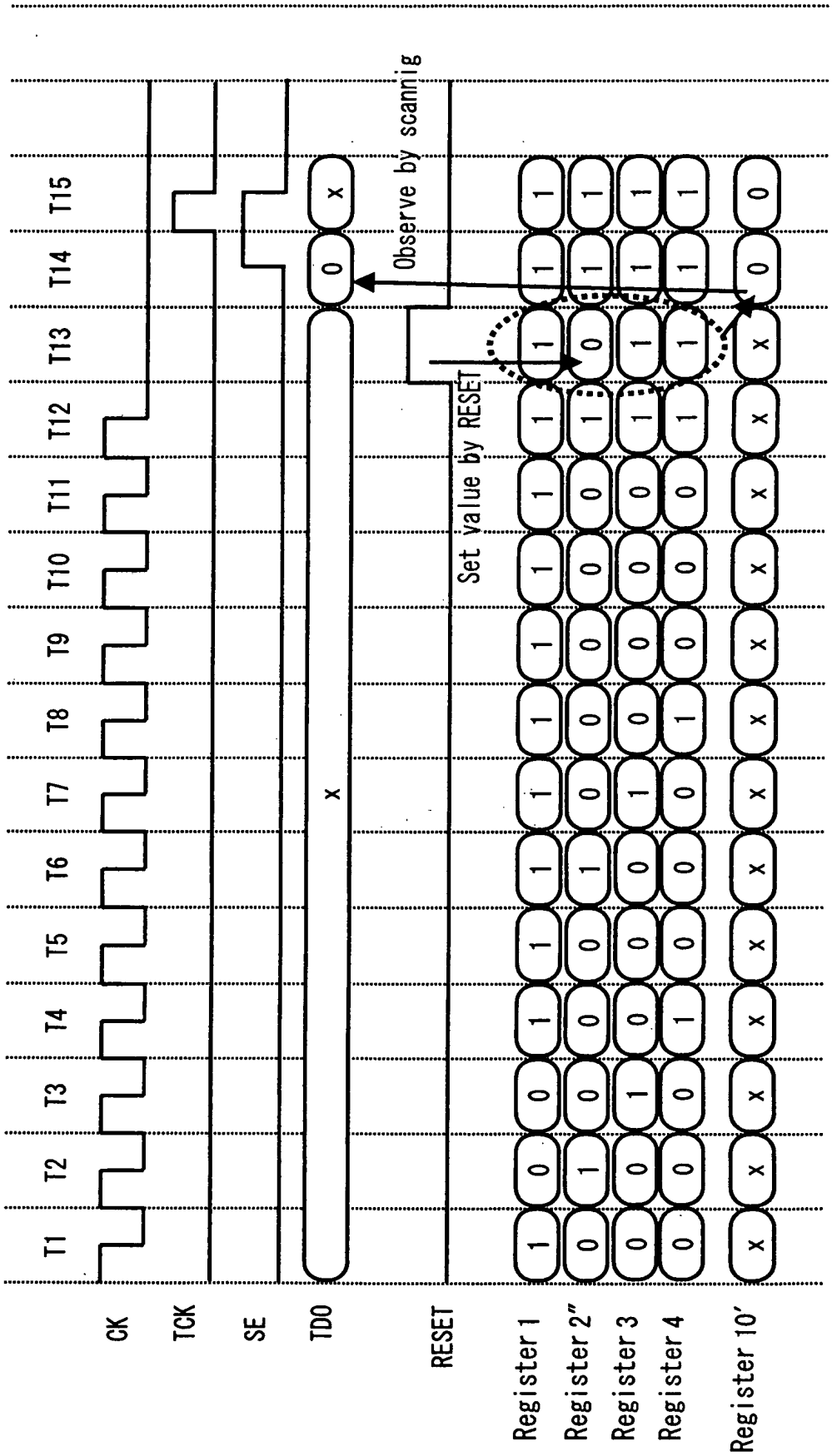

T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
CK
TCK
SE
TDO
RESET
Register 1
Register 2"
Register 3
Register 4
Register 10'
Observe by scannig
Set value by RESET

FIG. 9

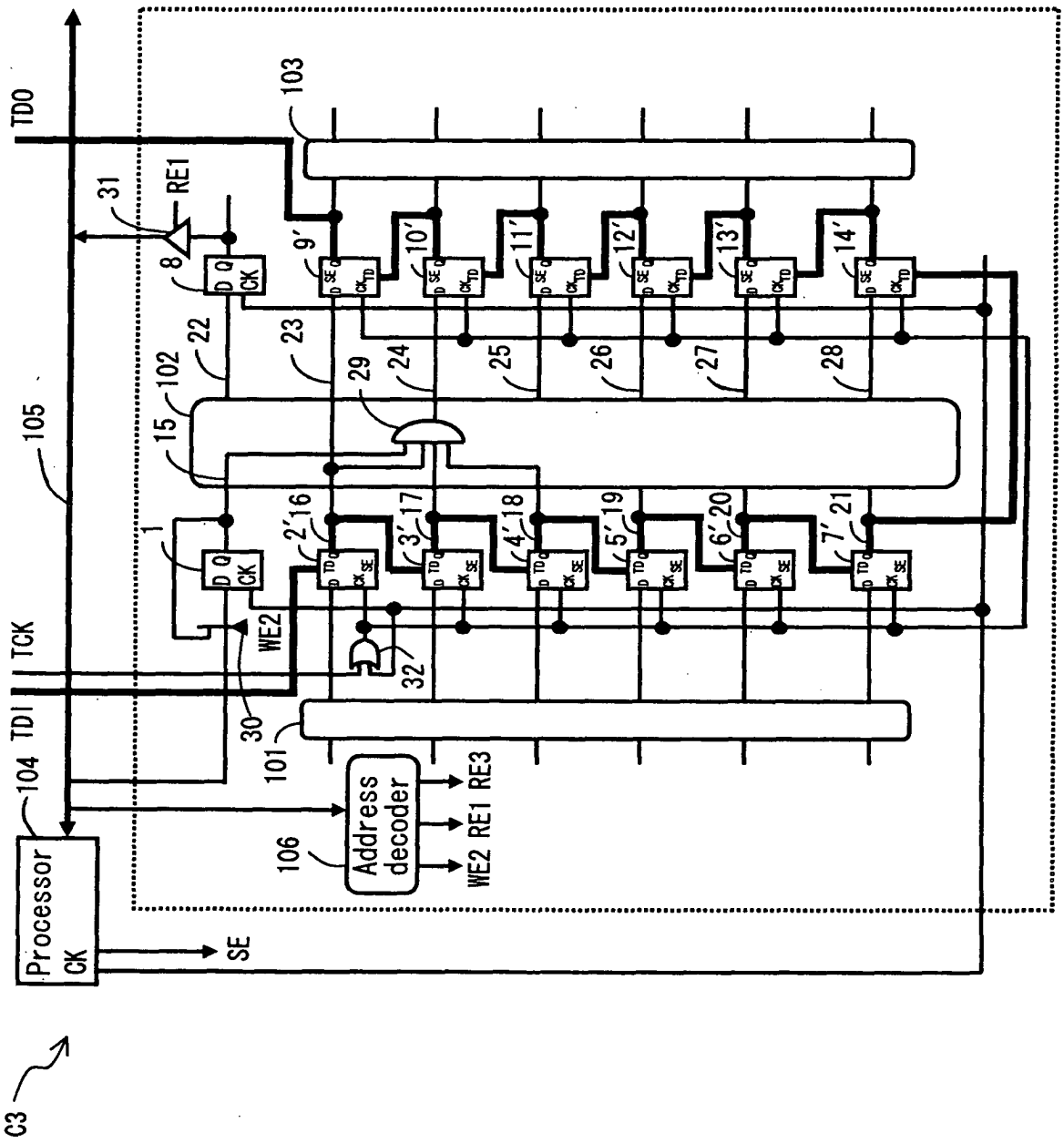

C3
Processor
CK
SE
TDO
TDI
TCK
RE1
WE2
Address decoder
WE2 RE1 RE3
101
102
103
104
105
106
1
2'
3'
4'
5'
6'
7'
8
9'
10'
11'
12'
13'
14'
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32

FIG. 10

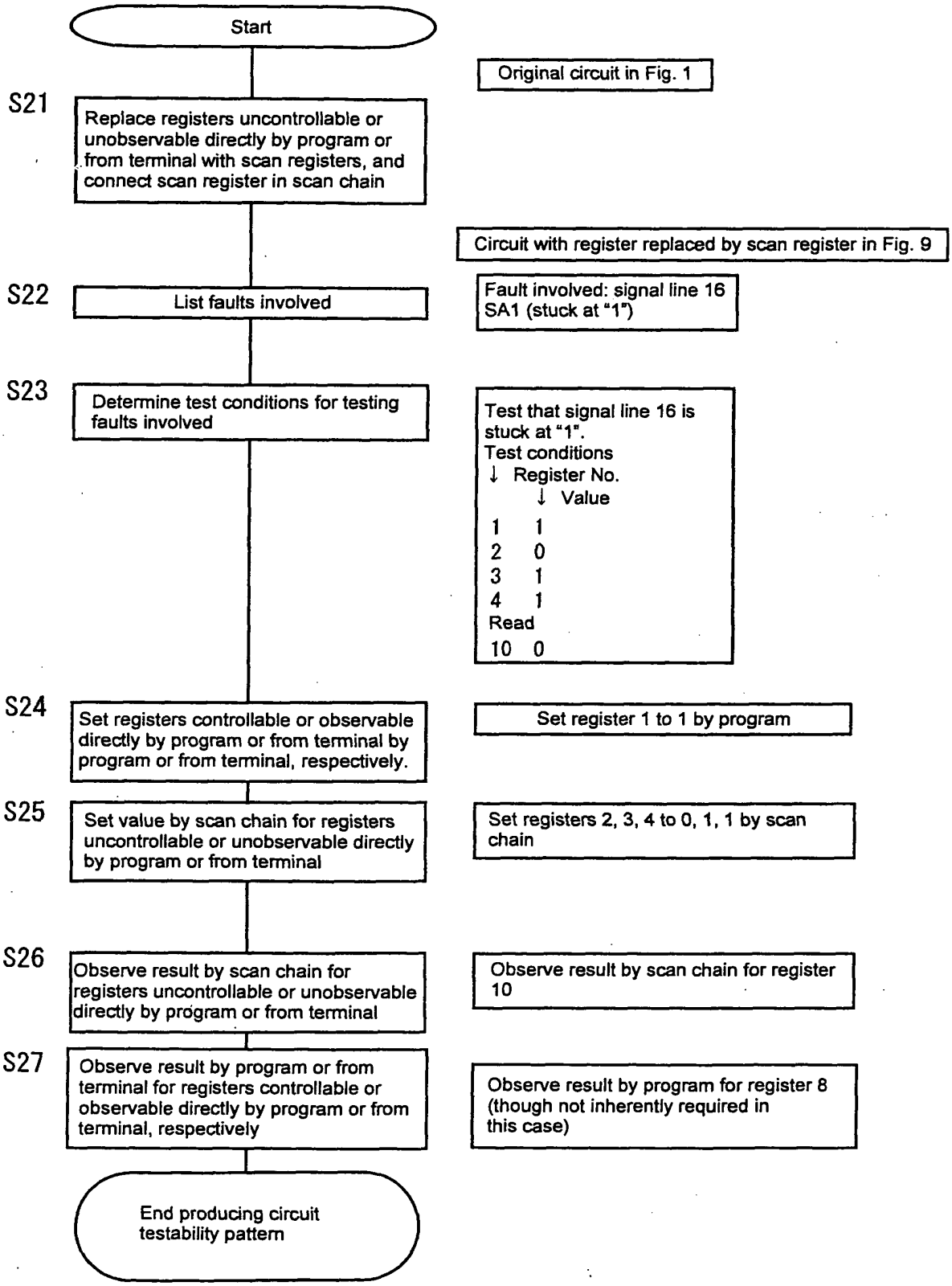

Start
Original circuit in Fig. 1
S21
Replace registers uncontrollable or unobservable directly by program or from terminal with scan registers, and connect scan register in scan chain
Circuit with register replaced by scan register in Fig. 9
S22
List faults involved
Fault involved: signal line 16 SA1 (stuck at "1")
S23
Determine test conditions for testing faults involved
Test that signal line 16 is stuck at "1".
Test conditions
↓ Register No.
↓ Value
1 1
2 0
3 1
4 1
Read
10 0
S24
Set registers controllable or observable directly by program or from terminal by program or from terminal, respectively.
Set register 1 to 1 by program
S25
Set value by scan chain for registers uncontrollable or unobservable directly by program or from terminal
Set registers 2, 3, 4 to 0, 1, 1 by scan chain
S26
Observe result by scan chain for registers uncontrollable or unobservable directly by program or from terminal
Observe result by scan chain for register 10
S27
Observe result by program or from terminal for registers controllable or observable directly by program or from terminal, respectively
Observe result by program for register 8 (though not inherently required in this case)
End producing circuit testability pattern

FIG. 11

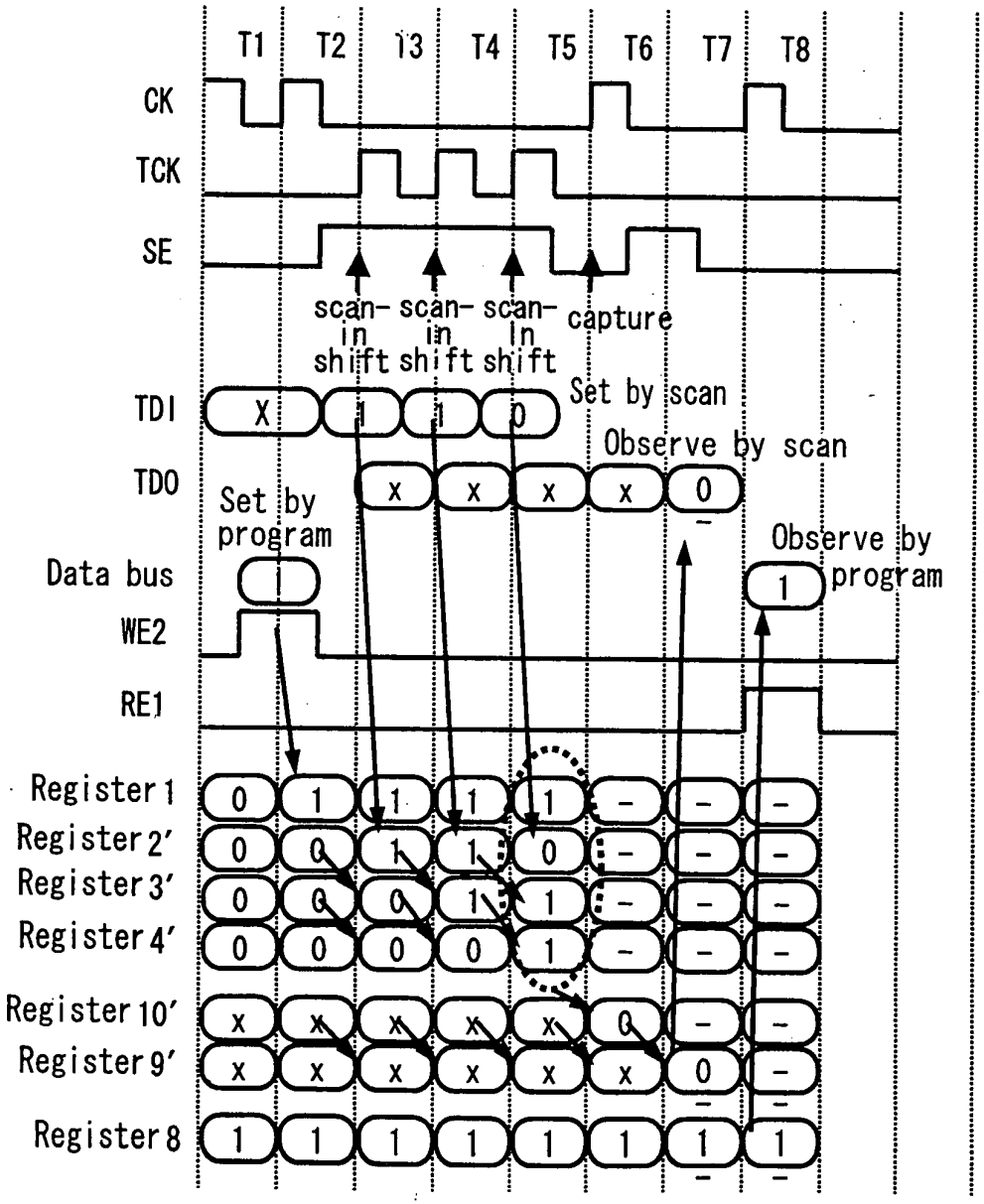
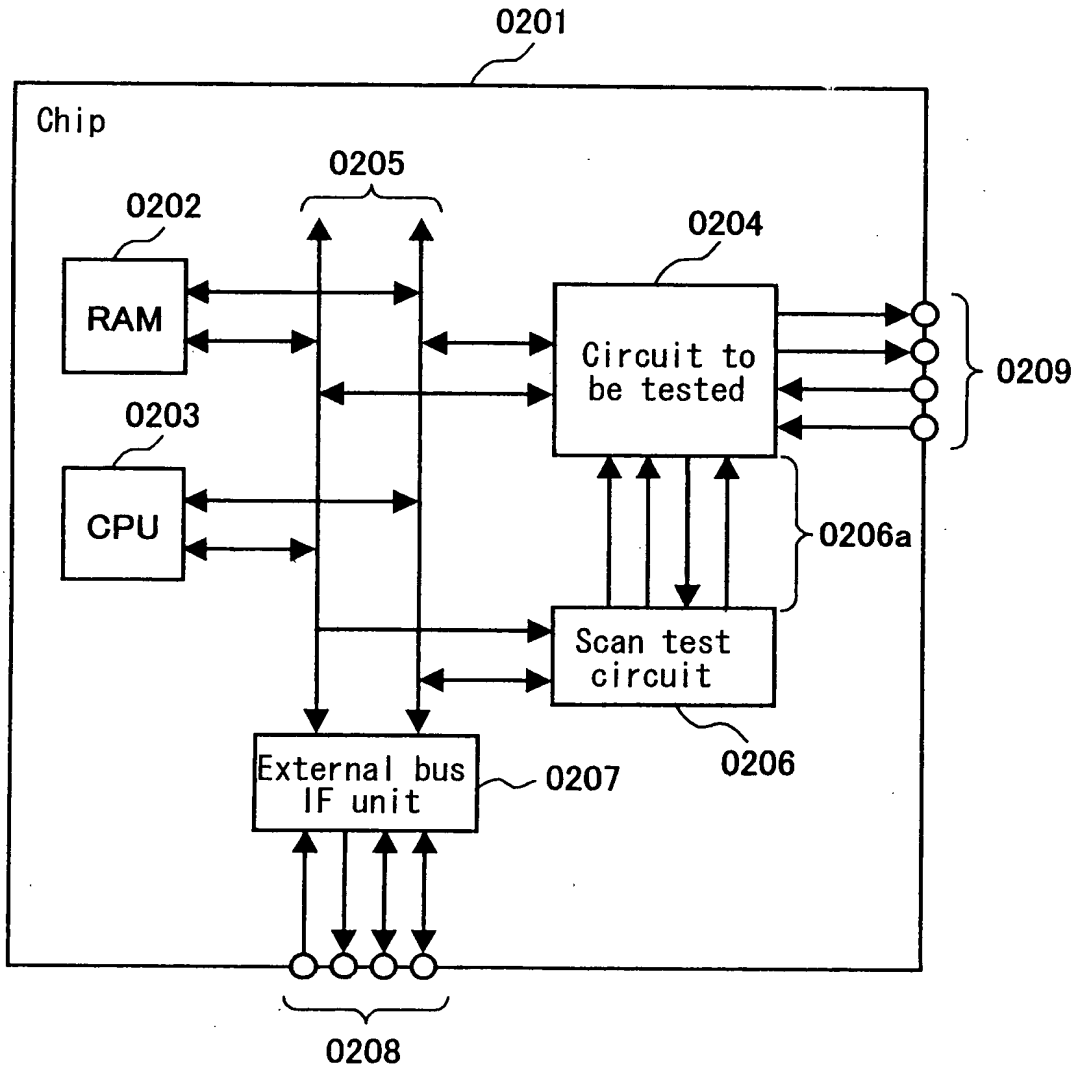

T1
T2
T3
T4
T5
T6
T7
T8
CK
TCK
SE
scan-in shift
scan-in shift
scan-in shift
capture
TDI
Set by scan
Observe by scan
TDO
Set by program
Observe by program
Data bus
WE2
RE1
Register 1
Register 2'
Register 3'
Register 4'
Register 10'
Register 9'
Register 8

FIG. 12


0201
Chip
0205
0202
0204
RAM
Circuit to be tested
0209
0203
CPU
0206a
Scan test circuit
External bus IF unit
0207
0206
0208